REMARKS

The claims are claims 1 to 11.

Claims 4 and 7 are amended to further distinguish over the cited reference.

Claims 1 to 7 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Dennin et al U.S. Patent No. 6,401,149 and Krakirian U.S. Patent No. 5,450,546.

Claims 1 and 5 recite subject matter not made obvious by the combination of Dennin et al and Krakirian. Claims 1 and 5 recite keeping two different counts for controlling access to the first-in-first-out buffer memory. Claim 1 recites "a master queue counter storing a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory," "decrement said master count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory" and "said master queue counter is further connected to said remote queue counter for incrementing said master count upon receipt of said decrement confirmation signal." Claim 5 recites "maintaining a master count indicative of a number of data entries available for data storage within a first-in-first-out buffer memory," "decrementing the master count upon allocation of data at the data source to be stored in the first-in-first-out buffer memory" and "incrementing the master count upon confirmation of decrementing of the remote count." The remote queue counter of claim 1 and the remote queue count of claim 5 is similar except that this is "indicative of a number of data entries within the first-in-first-out buffer memory currently storing data," incremented "upon allocation of data at said data source to be stored in said first-in-first-out buffer memory" and decremented "upon transfer of data out of the first-in-first-out buffer memory to the data destination." The OFFICE ACTION cites the second

counter at column 4 lines 19 to 36 and line 62 to column 5 line 16, 'block counter' column 7 lines 30 to 61 and column 8 lines 29 to 39 of Krakirian as disclosing using counters to monitor how full and empty is a FIFO buffer memory and minimize processor involvement thus improving performance.

The Applicants submit that the second counter/block counter 256 of Krakirian is not different than the FIFO utilization counter 414 of Dennin et al. Krakirian discloses at column 4, lines 27 to 36:

> "Preferably, the second counter is initialized to a predetermined value, for example, the minimum value or maximum value, and the first direction is towards the value opposite to the initialized value. Thus, if the second counter is initialized to the maximum value, the first direction is towards the minimum value. As each subsequent selected number of data segments are transferred to the buffer memory, the first counter generates the signal that changes the value of the second counter in the first direction."

When initialized to the maximum value, this second counter corresponds to the master queue counter of claim 1 and the master queue count of claim 5 storing a count indicative of the number of data entries available for storage. In this case, the second counter is decremented when "each subsequent selected number of data segments are transferred to the buffer memory." This corresponds to decrementing the master count as recited in claims 1 and 5. When initialized to the minimum value, this second counter corresponds to the remote queue counter of claim 1 and the remote count of claim 5 storing an indication of the number of FIFO entries storing data. In this case, the second counter is incremented when "each subsequent selected number of data segments are transferred to the buffer memory." This corresponds to incrementing the remote count as recited in claims 1 and 5. Thus as in the case of FIFO utilization counter 414 of Dennin et al,

Krakirian discloses a single counter or count and not the two counters recited in claim 1 nor the two counts recited in claim 5.

The first and third counters of Krakirian does not make obvious the other counter recited in claim 1 nor the other count recited in claim 5. The counts in the first and third counters of Krakirian are neither indicative of the number of data entries available for data storage nor the number of data entries currently storing data. Krakirian states at column 4, lines 19 to 26:

> "In one embodiment, the buffer room logic circuit of this invention includes a first counter for counting each data segment, typically a byte of data, transferred to the buffer memory. When the first counter has counted a selected number of data segments, typically a block of data, the first counter generates a signal that changes the value of a second counter in a first direction."

Krakirian also states at column 4, line 43 to 52:

> "However, data may also be transferred from the buffer memory, and in this embodiment, the buffer room logic circuit of this invention includes yet a third counter for counting each data segment, typically a byte of data, transferred from the buffer memory. When the third counter has counted a selected number of data segments, typically a block of data, the third counter generates a signal that changes the value of the second counter in a second direction opposite to the first direction."

These statements of Krakirian indicate that neither the first nor the third counter can indicate the number of data entries available for data storage or the number of data entries currently storing data. In particular, Krakirian teaches at column 7, lines 54 to 59 that host byte counter 254 rolls over upon reaching the specified count. Krakirian further teaches at column 8, lines 16 to 20 that disk byte counter 252 rolls over upon reaching the specified count. Upon such roll over any relationship between the counts in disk

byte counter 252 and host byte counter 254 to the number of data entries available for data storage or the number of data entries currently storing data is lost. The first counter/host byte counter 254 and the third counter/disk byte counter 252 merely divide the number of bytes transferred before the second counter/block counter 256 counts. Note further that Krakirian fails to teach that either the first or the third counter is decremented as both recited for the master queue counter and the remote queue counter of claim 1 and the master queue count and the remote queue count to claim 5. Thus Krakirian does not add anything to the teachings of Dennin et al to make obvious these recitations of claims 1 and 5. Accordingly, claims 1 and 5 are allowable over the combination of Dennin et al and Krakirian.

Dennin et al and Krakirian each disclose only a single counter where claims 1 and 5 require two. It is possible as a theoretical matter for a single reference structure to anticipate two claimed structures. However, in this instance the Applicant submits that the two claimed limitations cannot be anticipated by a single FIFO utilization counter 414 of Dennin et al or the single block counter 256 of Krakirian. Claims 1 and 5 recite different data is stored. Claims 1 and 5 recite "a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory" and "a remote count indicative of a number of data entries within said first-in-first-out buffer memory currently storing data." It is impossible for the single FIFO utilization counter 414 of Dennin et al or the single block counter 256 of Krakirian to store these different claimed amounts. Claims 1 and 5 recite different changes to the two counts on occurrence of the same event. Upon allocation of data to be stored in the first-in-first-out buffer memory, claim 1 recites "to decrement said master count" and "incrementing said remote count." Upon allocation of data to be stored in the first-in-first-out buffer memory, claim 5

recites "decrementing the master count" and "incrementing the remote count." On transfer of data out of the first-in-first-out buffer memory, claim 1 recites "decrementing said remote count and generating a decrement confirmation signal" and "incrementing said master count upon receipt of said decrement confirmation signal." On transfer of data out of the first-in-first-out buffer memory, claim 5 recites "decrementing said remote count" and "incrementing said master count upon confirmation of decrementing the remote count." Neither the single FIFO utilization counter 414 of Dennin et al nor the single block counter 256 of Krakirian can anticipate these opposite responses to the same event. This language clearly requires two counters in claim 1 and two counts in claim 5. Two counters/counts are required because the above quoted portions of the claims recite opposite results (increment/decrement) on the counters/counts in response to the same events. Neither the single FIFO utilization counter 414 of Dennin et al nor the single block counter 256 of Krakirian can both increment and decrement in response to allocation of data to the FIFO. The Applicants respectfully submit that the separate disclosure of single counters in Dennin et al and Krakirian cannot make obvious the two counters recited in claim 1 or the two counts recited in claim 5. Accordingly, claims 1 and 5 are allowable over the combination of Dennin et al and Krakirian.

Claims 2 and 6 recite subject matter not made obvious by the combination of Dennin et al and Krakirian. Claim 2 recites "said master queue counter is initialized to said predetermined number of data entries of said first-in-first-out buffer memory; and said remote queue counter is initialized at zero." Claim 6 recites "initializing the master count to the number of data entries of the first-in-first-out buffer memory; and initializing the remote count to zero." The OFFICE ACTION cites column 4, lines 19 to 36 and column 7, lines 30 to 61 of Krakirian as making obvious the

initialization of the master counter to the number of data entries in the buffer memory as recited in claim 2 and the initializing the master count to number of data entries in the buffer memory as recited in claim 6. However, claims 2 and 6 recite differing initialization of two counts. Dennin et al and Krakirian each disclose only one counter storing only one count. Because the single FIFO utilization counter 414 of Dennin et al and the single block counter 256 of Krakirian perform essentially the same function, these separate disclosures cannot make obvious the two initializations recited in claims 2 and 6. Accordingly, claims 2 and 6 are allowable over the combination of Dennin et al and Krakirian.

Claims 3 recites subject matter and claim 5 recites additional subject matter not made obvious by the combination of Dennin et al and Krakirian. Claim 3 recites "said data source may allocate data to said first-in-first-out buffer memory only if said master queue counter indicates a non-zero number of data entries available for data storage within said first-in-first-out buffer memory; and said data destination reads said first-in-first-out buffer memory only if said remote queue counter is non-zero." Claim 5 recites "allocating data from the data source to the first-in-first-out buffer memory only when the master count is non-zero," and "transferring data from the first-in-first-out buffer memory to the data destination only if the remote count is non-zero." The OFFICE ACTION cites column 4, lines 27 to 42 of Krakirian as teaching a data source may allocate data to a FIFO buffer memory only if a master queue counter indicates a non-zero number of data entries available for data storage within said FIFO buffer memory for the benefit of preventing buffer overflow. However, Krakirian states at column 4, lines 56 to 61:

> "If in this sequence, the second counter returns to the initialized value, the buffer memory is empty and the buffer room logic circuit generates a signal that stops data transfer from the buffer memory thereby preventing a data underrun without microprocessor intervention."

Thus Krakirian also states that the data transfer out of the FIFO buffer is also controlled by the count of the second counter. Since the data transfer is stopped when the second counter indicates the buffer memory is empty, data transfers out of the buffer memory occur only if the second counter does not indicate the buffer is empty. Claims 3 and 5 recite that this data transfer takes place "only if" the remote count is non-zero. Note that these two data transfer conditions are controlled by the two counters of claim 3 and the two counts of claim 5, whereas Krakirian teaches both these data transfers are controlled by the single second counter. Accordingly, claims 3 and 5 are allowable over the combination of Dennin et al and Krakirian.

Claims 4 and 7 recite subject matter not made obvious by the combination of Dennin et al and Krakirian. Claim 4 recites "said data source may selectively annul allocation of data of said data source to be stored in said first-in-first-out buffer memory for data allocated but whose transmission is annulled." Claim 7 recites "selectively annulling allocation of data of the data source to be stored in the first-in-first-out buffer memory for data allocated but whose transmission is annulled." The OFFICE ACTION cites the portion of Krakirian that teaches a master queue counter is connected to a data source that increments and decrements upon the receipt of a confirmation signal for monitoring how full and empty a FIFO buffer memory is, to benefit a system by minimizing processor involvement thus improving performance. However, this portion does not mention annulling allocation of data Amended claims 4 and 7 specifically recite that this annulling takes place for data allocated to be stored in the buffer memory

whose data transfer is annulled. Krakirian merely teaches stopping further data transfers and fails to teach annulling of an already allocated data location within the buffer memory. Accordingly, claims 4 and 7 are allowable over the combination of Dennin et al and Krakirian.

Claims 4 and 7 further recite subject matter not made obvious by the combination of Dennin et al and Krakirian. Claim 4 recites "said master queue counter is further connected to said data source to increment said master count upon receipt of said annul increment signal.." Claim 7 recites "incrementing the master count upon annulling allocation of data." The OFFICE ACTION fails to state where either Dennin et al or Krakirian teaches this subject matter. Krakirian fails to teach incrementing the master counter as recited in claim 4 or incrementing the master count as recited in claim 7 on blocking a data transfer. Accordingly, claims 4 and 7 are allowable over Dennin et al.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant request that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527